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EXAMINER	
AGGARWAL, YOGESH K	

ART UNIT	PAPER NUMBER
2615	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/772,267	LIU, TINA Y.	
	Examiner	Art Unit	
	Yogesh K. Aggarwal	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7* is/are allowed.

6)☐ Claim(s) *1,4,5,10* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1, 4, 5 and 10 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohzu et al. (US Patent # 6,747,699).

[Claim 1]

Ohzu et al. teaches a semiconductor imaging chip comprising:

an array of pixel sensors arranged in rows and columns, each of said pixels sensors having a respective pixel sensor signal value and a pixel sensor reset value (figure 26, S1, S2 and figure 27);

an output terminal (Vout);

a plurality of multiplexed column buffers, each of said plurality of multiplexed column buffers having a respective first plurality of input terminals coupled to a respective first plurality of said columns, each of-said plurality of multiplexed column buffers comprising:

first, second, third and fourth memory elements (Figure 26, capacitors Ct1, Ct2 and similar two capacitors shown connected to second column of the pixel array);

said first memory element adapted to store a pixel sensor signal value for a first column of said array (Ct1, col. 27 lines 19-29, figure 27 discloses the timing diagram);

said second memory element adapted to and a pixel sensor reset value for said first column of said array (Ct2);

said third memory element adapted to store a pixel sensor signal value for a second column of said array; said fourth memory element adapted to and a pixel sensor reset value for said second column of said array (similar two capacitors shown connected to second column of the pixel array);

a differential gain amplifier having respective first and second input terminals and a respective output terminal (figure 26, differential gain amplifier 723A);

said first input terminal of said differential gain amplifier being selectively coupled to one of said first and third memory elements (721A);

said second input terminal of said differential gain amplifier being selectively coupled to one of said second and fourth memory elements (722A); and

the output terminal of said differential gain amplifier being selectively coupled to said output terminal of said semiconductor imaging chip (Vout).

Ohzu fails to teach if the pixel sensors are an APS array. However Official Notice is taken of the fact that it is very well known in the art to have an APS array in order to have low read noise comparable to other pixel systems. Therefore taking the combined teachings of Ohzu and Official Notice, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have an APS array in order to have low read noise comparable to other pixel systems.

[Claim 4]

Ohzu et al. teaches a semiconductor imaging chip comprising:

an array of pixel sensors arranged in rows and columns a plurality of multiplexed column buffers each of said plurality of column buffers being coupled to a group of columns (figure 26, S1, S2 and figure 27), each of said plurality of column buffers comprising:

respective first, second, third and fourth memory elements (Figure 26, capacitors Ct1, Ct2 and similar two capacitors shown connected to second column of the pixel array);

respective first, second, third, fourth, fifth, sixth, seventh and eighth switches (Transistors Qt1, Qt2, Qs1, Qs2 and similar four switches shown connecting second column of the pixel array to two capacitors shown in the second column of the pixel array);

a differential gain amplifier having respective first and second input terminals and a respective output terminal (723A);

said first switch coupling said first memory element to a first column of said array of pixel sensors (Qt1 couples Ct1 to first column of the pixel array);

said second switch coupling said second memory element of said first column of said array of pixel sensors (Qt2 couples Ct2 to said first column of the pixel array);

said third switch coupling said third memory element to a second column of said array of pixel sensors; said fourth switch coupling said fourth memory element to said second column of said array of pixel sensors (similar two transistor switches shown connecting second column of the pixel array to two capacitors shown in the second column of the pixel array);

said fifth and sixth switches coupling said first and third memory elements to said first input terminal of said differential gain amplifier respectively; said seventh and eighth switches

coupling said second and fourth memory element to said second input terminal of said differential gain amplifier (Qs1 and similar transistor in the second column connected to bus 721A and to first input terminal of differential amplifier 723A. Similarly Qs2 and a transistor in the second column connected to bus 722A and to second input terminal of differential amplifier 723A).

Ohzu fails to teach if the pixel sensors are an APS array. However Official Notice is taken of the fact that it is very well known in the art to have an APS array in order to have low read noise comparable to other pixel systems. Therefore taking the combined teachings of Ohzu and Official Notice, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have an APS array in order to have low read noise comparable to other pixel systems.

[Claim 10]

Ohzu et al. teaches a semiconductor imaging chip comprising

an array of pixel sensors arranged in rows and columns (figure 26, S1, S2 etc.);

an output terminal (Vout);

a first multiplexed column buffer having a first pattern cancellation circuit for providing a first corrected APS pixel signal value formed by the difference between an APS pixel signal value and an APS pixel reset value (col. 27 lines 17-40),

said first multiplexed column buffer having at least two input terminals coupled to a first column and a second column respectively of said array of pixel sensors, said first multiplexed column buffer having a respective output terminal to sequentially provide a corrected APS pixel signal value for said first column and a corrected APS pixel signal value for said second column

(VL1 and VL2 comprise at least two input terminals coupled to a first column and a second column respectively of said array of pixel sensors, col. 27 lines 27-40 and the timing diagram of figure 27);

a second multiplexed column buffer having a second pattern cancellation circuit for providing a second corrected APS pixel signal value formed by the difference between an APS pixel signal value and an APS pixel reset value (col. 27 lines 17-40),

said second multiplexed column buffer having at least two input terminals coupled to a third column and a fourth column respectively of said array of pixel sensors, said second multiplexed column buffer having a respective output terminal to sequentially provide a corrected APS pixel signal value for said second column and a corrected APS pixel signal value for said fourth column (See Examiner notes above); and

said output terminal of said first multiplexed column buffers being sequentially coupled to said output terminal of said semiconductor imaging chip and said output terminal of said second multiplexed column buffers being sequentially coupled to said output terminal of said semiconductor imaging chip so as to sequentially readout corrected APS pixel-signal values for first, second, third and fourth columns of said array of pixel sensors at said output terminal (See figure 26 and 27).

Ohzu fails to teach if the pixel sensors are an APS array. However Official Notice is taken of the fact that it is very well known in the art to have an APS array in order to have low read noise comparable to other pixel systems. Therefore taking the combined teachings of Ohzu and Official Notice, it would be obvious to one skilled in the art at the time of the invention to

have been motivated to have an APS array in order to have low read noise comparable to other pixel systems.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohzu et al. (US Patent # 6,747,699) in view of Egawa et al. (US Patent # 6,801,256).

[Claim 5]

Claim 5 is a combination of claims 1 and 4 except a bus driver amplifier having respective input and output terminals and said output terminal of said bus driver amplifier being selectively coupled to said output bus terminal of said imaging chip to sequentially readout corrected pixel sensor values for said first and second columns. However Egawa et al. teaches an output amplifier 27 (figure 1) in order to amplify signals from the photoelectric conversion on the output signal line in order to raise their signal strength and intensity. Therefore taking the combined teachings of Ohzu and Egawa, it would be obvious to one skilled in the art at the time of the invention to have been motivated to have a bus driver amplifier as taught in Egawa to be used in the system of Ohzu chip to sequentially readout corrected pixel sensor values for said first and second columns in order to amplify signals from the photoelectric conversion on the output signal line in order to raise their signal strength and intensity.

Allowable Subject Matter

5. Claim 7 is allowed.

See previous office action for reasons of allowance.

6. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art fails to show said fifth memory element being selectively

coupled to .. , said sixth memory element being selectively coupled to...., said input terminal of said multiplexed bus driver ....

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yogesh K. Aggarwal whose telephone number is (571) 272-7360. The examiner can normally be reached on M-F 9:00AM-5:30PM.

8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)-272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

YKA
January 16, 2006

DAVID OMETZ
SUPERVISORY PATENT EXAMINER